UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/954,515	09/17/2001	Hyung-Chul Choi	M0023/7000D	9063

22832 7590 04/03/2006

KIRKPATRICK & LOCKHART NICHOLSON GRAHAM LLP
STATE STREET FINANCIAL CENTER
ONE LINCOLN STREET
BOSTON, MA 02111-2950

EXAMINER	
HON, SOW FUN	

ART UNIT	PAPER NUMBER
1772	

DATE MAILED: 04/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/954,515	CHOI ET AL.	
	Examiner	Art Unit	
	Sow-Fun Hon	1772	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-24 and 26-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-24 and 26-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/09/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Withdrawn Rejections

1. The 35 U.S.C. 103(a) rejections of claims 18-24,26-32 over Fukuyoshi as the primary reference, are withdrawn due to Applicant's amendment dated 01/10/06.

Repeated Rejections

2. The 35 U.S.C. 112, 1st paragraph rejection of claims 29-32 are repeated for the same reasons previously of record in the Office action dated 08/09/05.

3. The 35 U.S.C. 103(a) rejections of claims 29-31 over Fukuyoshi in view of CERAC, as the primary combination, are repeated for the same reasons previously of record in the Office action dated 08/09/05.

New Rejections

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 18, 24, 26, 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Austin (US 5,508,091).

Regarding claims 18, 24, Austin teaches a transparent electrode assembly (column 3, lines 21-25) in Fig. 16, shown on the next page, comprising: a substrate (22,

column 11, line 22); a high index layer formed on the substrate (108, silicon nitride, column 16, lines 18-19, refractive index of layer 109 is less than the refractive index of layer 108, column 16, lines 13-16); a conductive layer formed on the high index layer (electrically conductive layer 106, column 16, lines 21-24); and a high index top layer (104, silicon nitride, column 16, lines 18-19, high refractive index layer outermost, abstract), having a thickness of 23 nm (first layer 104, column 16, line 18, Layer No. 1, column 16, lines 40-41), which is within the claimed range of from about 20 nm to about 100 nm, or from about 20 nm to less than about 30 nm, formed on the conductive layer (electrically conductive layer 106, column 16, lines 21-24), at least the top layer and the conductive layer being patterned so as to divide the conductive layer into a plurality of discrete electrodes (patterned, column 4, lines 52-53, plurality of spaced apart electrodes, column 4, lines 1-5), and a layer of silica (109 is a layer of silicon dioxide, column 16, lines 17-18) disposed on the substrate (22, column 11, line 22), the layer of silica 109 in substantially continuous contact with the substrate 22, as shown in Fig. 16 below.

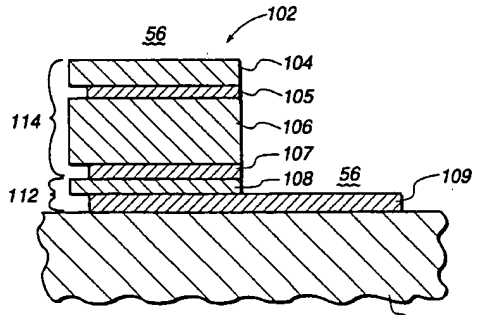


Fig. 16

Austin fails to disclose the conductivity of high index top layer 104.

However, Austin teaches that high index layer 104 can include titanium dioxide and tin dioxide which are materials disclosed by Applicant's specification (original claim 24), in place of the silicon nitride in the examples, and that the multilayer coating 114 comprising high index layer 104, may have a conductivity, as defined by Applicant, of between about 2 and 200 ohms/square (column 3, lines 65-66), which overlaps the claimed range of from about 100 to 400 ohms/square.

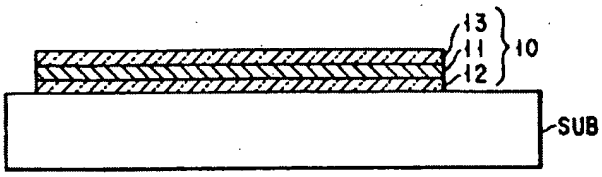
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to have used a high index top layer having a conductivity within the range of from about 100 to about 400 ohms/square, as the high index top layer of the electrode assembly of Austin, in order to utilize the combination of high index and specific conductivity for the top layer, as taught by Austin.

Regarding claim 26, Austin teaches a liquid crystal display assembly comprising a liquid crystal material sandwiched between two electrode assemblies (electrode-coated sheets, column 2, lines 1-5), and that the electrode assembly as described above is used in the liquid crystal display assembly (column 3, lines 20-25).

Regarding claim 32, Austin teaches that the layer of silica has a thickness of about 25 nm (layer 109 is a layer of silicon dioxide, column 16, lines 17-19), which is within the claimed range of from about 10 to about 30 nm.

4. Claims 18-24, 26-27, 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuyoshi (US 5,667,853) in view of CERAC (CERAC Technical Publications) and Austin (US 5,508,091).

Regarding claims 18, 32, Fukuyoshi teaches an electrode assembly (multilayered conductive film), in Fig. 1 on the next page, comprising a substrate (SUB); a first transparent oxide layer 12 formed on the substrate; a silver-based metallic layer 11 formed on transparent oxide layer 12; and a second transparent layer 13 formed on the conductive layer 11 (column 4, lines 20-30). The silver layer 11 is conductive (column 5, lines 55-60). Layers 12 and 13 are high refractive index layers (column 12, lines 1-10).



Fukuyoshi teaches that the resist film of the predetermined electrode pattern is formed on the transparent oxide layer 13, and that the electrode pattern is etched with the three thin layers aligned with each other, forming transparent multilayered conductive films of electrodes (column 13, lines 45-55). Hence at least the top transparent oxide layer 13 and the conductive layer 11 are patterned so as to divide the conductive layer into a plurality of discrete electrodes.

Fukuyoshi teaches that the top transparent oxide layer 13 has a thickness of 30 to 100 nm (column 5, lines 25-30), which overlaps the claimed range of about 20 nm to about 100 nm. Fukuyoshi teaches that the high index top transparent oxide layer 13 comprises primarily indium oxide (column 6, lines 60-65) and a small amount of tin oxide (forming indium tin oxide), titanium (di)oxide or gallium oxide to adjust the

conductivity (column 7, lines 20-30), but fails to disclose that it has a conductivity ranging from about 100 ohms/square to about 400 ohms/square.

However, CERAC teaches that high conductivity is balanced against high transmission in the visible light region, and that indium tin oxide must have a conductivity (in Applicant's terminology) or sheet resistance of greater than 100 ohms/square in order to obtain visible region transmission near 90 % (Film Properties section), wherein an application is for electrodes (Introduction section).

Therefore, it would have been obvious for one of ordinary skill in the art at the time the invention was made, to have used indium tin oxide with a conductivity ranging from about 100 ohms/square to about 400 ohms/square, as the high index transparent oxide top layer of Fukuyoshi, in order to obtain a conductive electrode with high transmission in the visible light region, as taught by CERAC.

Fukuyoshi fails to teach a layer of silica disposed on the substrate in substantially continuous contact with the substrate, let alone its thickness.

However, Austin teaches a layer of silica in continuous contact with the substrate (barrier layer 54 of silicon dioxide, deposited on substrate 22, column 11, lines 20-27), with a thickness of about 25 nm (layer 109 is a layer of silicon dioxide, column 16, lines 17-19), which is within the claimed range of from about 10 to about 30 nm, for the purpose of preventing material from substrate 22 from diffusing into other layers of the coating (column 12, lines 16-23) for a transparent electrode assembly (column 1, lines 14-19).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to have provided a barrier layer of silica disposed in continuous contact with the substrate in the transparent electrode assembly of Fukuyoshi, in order to prevent material from the substrate from diffusing into the other layers, as taught by Austin.

Regarding claim 19, Fukuyoshi in view of CERAC and Austin, fails to teach that the electrode assembly has a plurality of conductors connected to portions of the top layer overlying the discrete electrodes.

However, Fukuyoshi teaches a chip for driving the device formed overlying (on) a portion of the electrode (column 10, lines 25-35). Contacts, which are conductors, are needed for the purpose of connecting the electrodes to the chip.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to have used a plurality of conductors connected to portions of the top layer overlying the discrete electrodes in the electrode assembly of Fukuyoshi in view of CERAC and Austin, in order to provide electrical contacts connecting the electrodes to the chip, as taught by Fukuyoshi.

Regarding claim 20, Fukuyoshi in view of CERAC and Austin, fails to teach that the high index layer adjacent the substrate is an electrically insulating layer.

However, Fukuyoshi teaches a set of electrodes 34 that is adjacent to the screen (user)-side substrate 31 in Fig. 3 (column 9, lines 14-24). The layer that is adjacent to the substrate with the potential of contacting the observer would need to be electrically insulating for the purpose of preventing any electrical shock to the user.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to have made the high index layer, which is adjacent to the screen-side substrate, of Fukuyoshi in view of CERAC and Austin, an electrically insulating one, in order to protect the user from electrical shock.

Regarding claim 21, Fukuyoshi teaches that the substrate is a synthetic resin material (plastic, column 9, lines 40-50).

Regarding claims 22, 24, Fukuyoshi teaches that the high index top transparent oxide layer 13 comprises primarily indium oxide (column 6, lines 60-65) and a small amount of tin oxide (forming indium tin oxide), titanium (di)oxide or gallium oxide to adjust the conductivity (column 7, lines 20-30).

Regarding claim 23, Fukuyoshi teaches that the conductive layer 11 comprises silver and gold (column 5, lines 45-55) which form an alloy.

Claim 24 has been discussed above.

Regarding claim 26, Fukuyoshi teaches a liquid crystal display assembly comprising a liquid crystal material LC sandwiched (column 9, lines 49-50) between two electrode assemblies 42 and 34 in Fig. 3 (column 9, lines 35-40).

Regarding claim 27, Fukuyoshi in view of CERAC and Austin, fails to teach that the liquid crystal display screen (column 21, lines 20-25) is a touch screen-type.

However, touch screen displays were notoriously well known to one of ordinary skill in the art at the time the invention was made, for the purpose of providing touch-screen capability.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to have made the liquid crystal display screen of Fukuyoshi into a touch-screen-type, in order to provide the desired touch-screen capability.

5. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuyoshi in view of CERAC and Austin, as applied to claims 18-24, 26-27, 32 above, and further in view of Yatabe (US 4,234,654).

Fukuyoshi in view of CERAC and Austin, teaches a substantially transparent electrode assembly comprising: a substrate; a high index layer formed on the substrate; a conductive layer formed on the high index layer; a high index top layer having a conductivity ranging from about 100 ohms/square to about 400 ohms/square and a thickness within the range of from about 20 nm to about 100 nm, formed on the conductive layer, at least the top layer and the conductive layer being patterned so as to divide the conductive layer into a plurality of discrete electrodes, and a layer of silica disposed on the substrate, the layer of silica in a substantially continuous contact with the substrate, as discussed above.

In addition, Fukuyoshi teaches that the substrate is a synthetic resin (plastic) material (column 9, lines 40-50), but fails to disclose the species.

However, Yatabe teaches a conductive laminate used as a transparent electrode structure for a liquid crystal display (column 9, lines 20-30), wherein the substrate material may be polycarbonate, or polyacrylate (acrylic resin) (column 7, lines 55-65) for the purpose of utilizing the physical properties of said materials.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to have used polycarbonate or polyacrylate as materials for the synthetic resin substrate in the electrode assembly of Fukuyoshi in view of CERAC and Austin, in order to take advantage of the physical properties of said synthetic resins, as taught by Yatabe.

Response to Arguments

7. Applicant's arguments regarding the new limitation of "layer of silica in substantially continuous contact with the substrate", with respect to claims 18-24, 26-28, 32 have been considered but are moot in view of the new ground(s) of rejection. However, relevant arguments regarding the valid combination of Fukuyoshi and CERAC are addressed below.

8. Applicant argues that the present specification states that the preferred materials and processes for forming the top layer are the same as those for forming the insulating layer, except that the condition used to deposit the top layer should be varied so as to give the top layer substantial conductivity, while CERAC fails to teach or suggest

varying the condition used to deposit the high index top layer and the high index [intermediate layer].

Applicant is respectfully apprised that CERAC teaches that high conductivity is balanced against high transmission in the visible light region, and that indium tin oxide must have a conductivity (in Applicant's terminology) or sheet resistance of greater than 100 ohms/square in order to obtain visible region transmission near 90 % (Film Properties section), wherein an application is for electrodes (Introduction section). CERAC's teaching of the need to balance conductivity versus visible region transmission provides the motivation to vary the condition used to deposit the high index top layer and the high index intermediate layer, for the purpose of providing the desired balance of conductivity and visible region transmission for the layer as related to its position in the electrode assembly of Fukuyoshi. Furthermore, even though product by process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. See MPEP 2113 [R-1].

9. Applicant's arguments regarding the 35 U.S.C. 112, 1st paragraph rejection of claims 29-31, have been fully considered but they are not persuasive. There are no examples or specific numerical recitation in the specification to support the new limitation restricting the range to the upper limit of less than about 30 nm. See MPEP 2163.05 [R-2] III.

10. Applicant's arguments regarding the 35 U.S.C. 103(a) rejections of claims 29-31 over Fukuyoshi in view of CERAC have been fully considered but they are not persuasive. Applicant argues that the fact that Fukuyoshi does not teach away from using a lower thickness value, fails to establish a prima facia basis for an obviousness rejection.

Applicant is respectfully reminded that while Fukuyoshi teaches a lower limit of 30 nm (column 5, lines 25-30), Fukuyoshi does not teach against a lower thickness value for a smaller electrode assembly. Applicant is respectfully apprised that the change in proportion/size is not an indication of patentability in itself. See MPEP 2144.04 [R-1] IV A. US 5,508,091(column 16, lines 18-19, 40-41, lines 51-54) is evidence that the feature is not patentable in itself.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication should be directed to Sow-Fun Hon whose telephone number is (571)272-1492. The examiner can normally be reached Monday to Friday from 10:00 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Harold Pyon, can be reached at (571)272-1498. The fax phone number for the organization where this application or proceeding is assigned is (571)273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S. Hon

Sow-Fun Hon

03/27/06

HAROLD PYON
SUPERVISORY PATENT EXAMINER
1772

3/29/06